

DATA SHEET

74LV4060

14-stage binary ripple counter with
oscillator

Product specification

1998 Jun 23

14-stage binary ripple counter with oscillator

74LV4060

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for Low Voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_{amb} = 25^{\circ}\text{C}$.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_{amb} = 25^{\circ}\text{C}$.
- All active components on chip
- RC or crystal oscillator configuration
- Output capability: standard (except for R_{TC} and C_{TC})
- I_{CC} category: MSI

APPLICATIONS

- Control Counters
- Timers
- Frequency Dividers
- Time-delay circuits

DESCRIPTION

The 74LV4060 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT4060.

The 74LV4060 is a 14-stage ripple-carry counter/divider and oscillator with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (Q_3 to Q_9 and Q_{11} to Q_{13}) and an overriding asynchronous master reset (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case, keep the oscillator pins (R_{TC} and C_{TC}) floating.

The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q_3 to Q_9 and Q_{11} to $Q_{13} = \text{LOW}$), independent of the other input conditions.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay RS to Q_3	$C_L = 15$ pF $V_{CC} = 3.3$ V	29	ns
t_{PHL}	Q_n to Q_{n+1}		6	
	MR to Q_n		16	
f_{max}	Maximum clock frequency		99	MHz
C_1	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per package	Notes 1, 2 and 3	40	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_1 = \text{GND}$ to V_{CC}
3. For formula on dynamic power dissipation, see the following pages.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	-40°C to $+125^{\circ}\text{C}$	74LV4060 N	74LV4060 N	SOT38-4
16-Pin Plastic SO	-40°C to $+125^{\circ}\text{C}$	74LV4060 D	74LV4060 D	SOT109-1
16-Pin Plastic SSOP Type II	-40°C to $+125^{\circ}\text{C}$	74LV4060 DB	74LV4060 DB	SOT338-1
16-Pin Plastic TSSOP Type I	-40°C to $+125^{\circ}\text{C}$	74LV4060 PW	74LV4060PW DH	SOT403-1

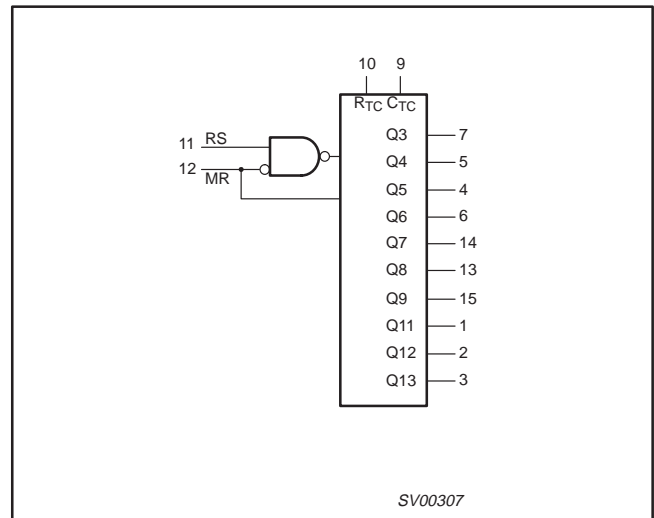
14-stage binary ripple counter with oscillator

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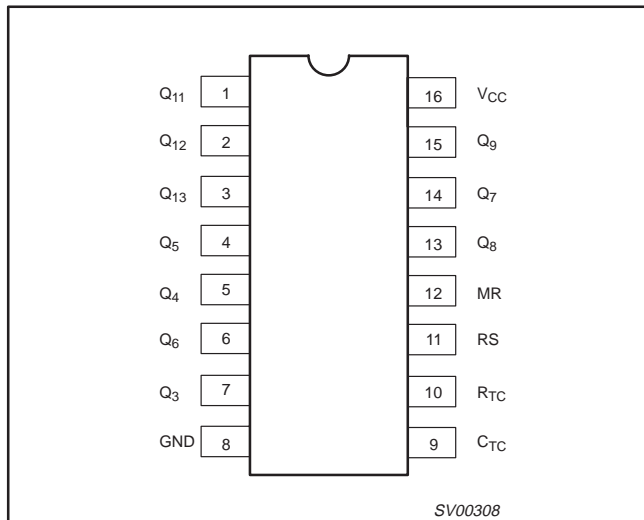
PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1, 2, 3	Q ₁₁ to Q ₁₃	Counter outputs
7, 5, 4, 6, 15, 13, 15	Q ₃ to Q ₉	Counter outputs
8	GND	Ground (0 V)
9	C _{TC}	External capacitor connection
10	R _{TC}	External resistor connection
11	RS	Clock input/oscillator pin
12	MR	Master reset
16	V _{CC}	Positive supply voltage

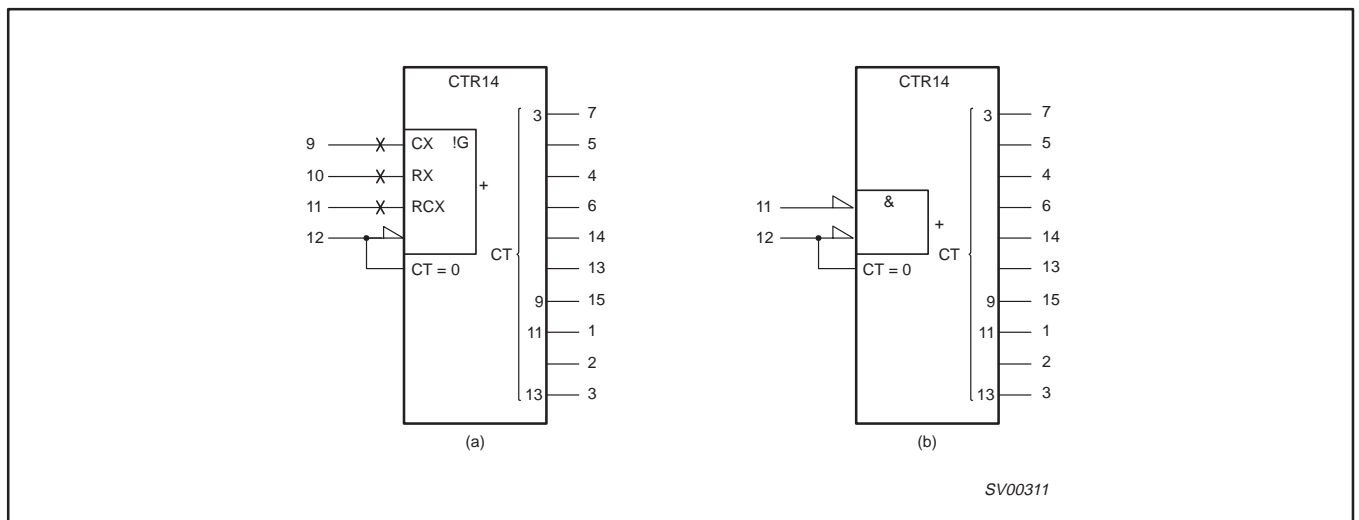
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



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DYNAMIC POWER DISSIPATION

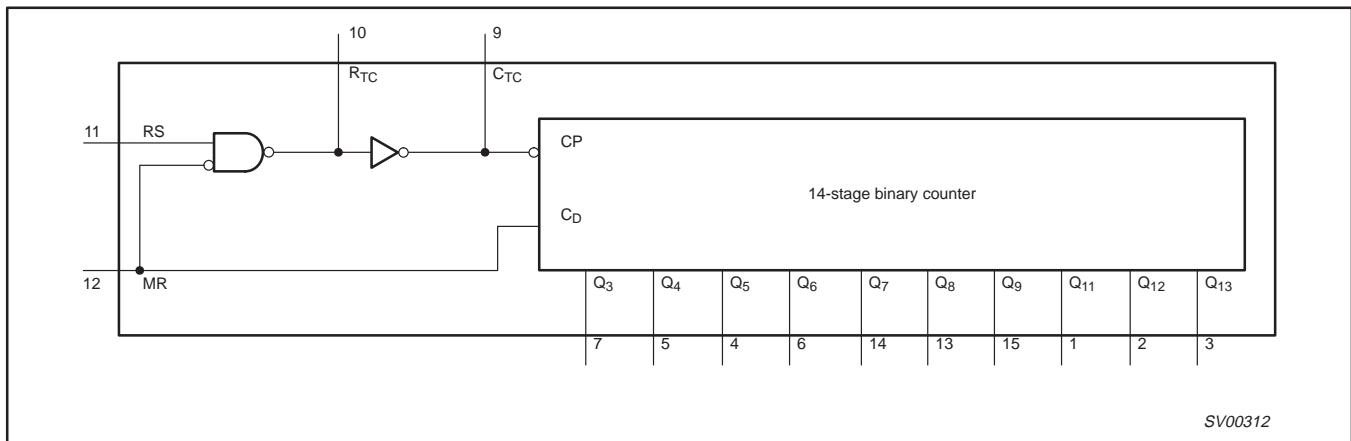
GND = 0 V; T_{amb} = 25 °C

PARAMETER	V _{CC} (V)	TYPICAL FORMULA FOR P _D (μW) ¹
Total dynamic power dissipation when using the on-chip oscillator (P _D)	1.2	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 16 \times V_{CC}$
	2.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 460 \times V_{CC}$
	3.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1000 \times V_{CC}$

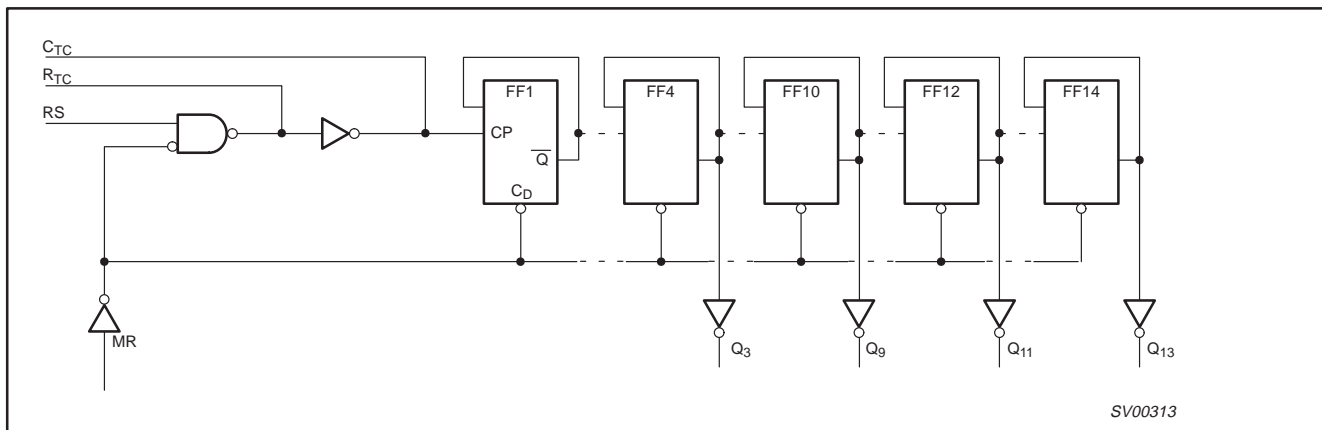
NOTE:

- Where: f_o = output frequency in MHz; f_{osc} = oscillator frequency in MHz;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs; C_L = output load capacitance in pF;
 C_t = timing capacitance in pF; V_{CC} = supply voltage in V.

FUNCTIONAL DIAGRAM



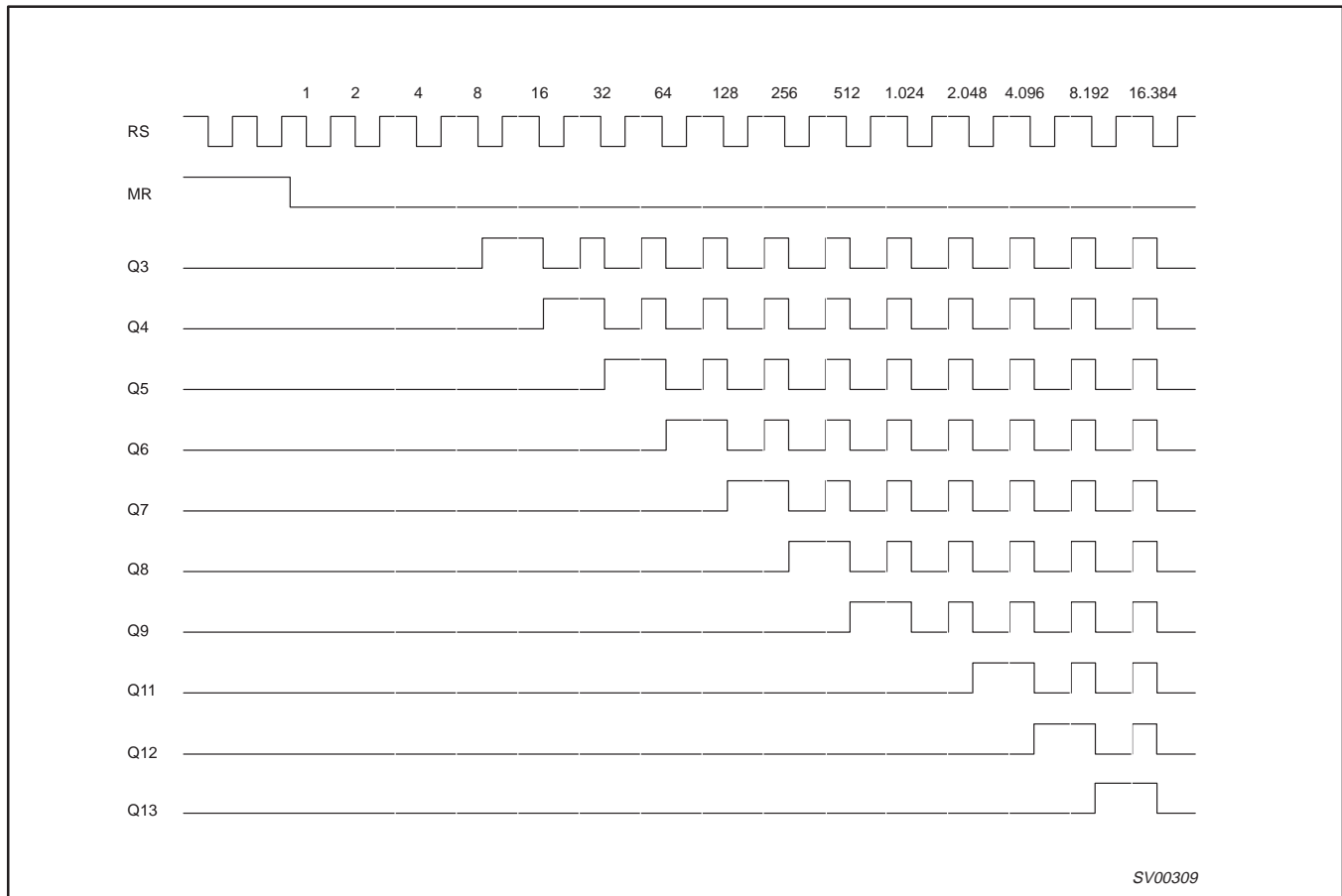
LOGIC DIAGRAM



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TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134)
 Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current - standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND},$ $\pm I_{CC}$	DC V_{CC} or GND current for types with -standard outputs		50	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package -plastic DIL -plastic mini-pack (SO) -plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note ¹	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$ $V_{CC} = 3.6V$ to $5.5V$	– – – –	– – – –	500 200 100 50	ns/V

NOTES:

1. The LV is guaranteed to function down to $V_{CC} = 1.0V$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2V$ to $V_{CC} = 5.5V$.

DC CHARACTERISTICS

Over operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			–40°C to +85°C			–40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage MR input	$V_{CC} = 1.2V$	0.9	–	–	0.9	–	V
		$V_{CC} = 2.0V$	1.4	–	–	1.4	–	
		$V_{CC} = 2.7$ to $3.6V$	2.0	–	–	2.0	–	
		$V_{CC} = 4.5$ to $5.5V$	$0.7 * V_{CC}$	–	–	$0.7 * V_{CC}$	–	
V_{IL}	LOW level Input voltage MR input	$V_{CC} = 1.2V$	–	–	0.3	–	0.3	V
		$V_{CC} = 2.0V$	–	–	0.6	–	0.6	
		$V_{CC} = 2.7$ to $3.6V$	–	–	0.8	–	0.8	
		$V_{CC} = 4.5$ to 5.5	–	–	$0.3 * V_{CC}$	–	$0.3 * V_{CC}$	
V_{IH}	HIGH level Input voltage RS input	$V_{CC} = 1.2V$	1.0	–	–	1.0	–	V
		$V_{CC} = 2.0V$	1.6	–	–	1.6	–	
		$V_{CC} = 2.7$ to $3.6V$	2.4	–	–	2.4	–	
		$V_{CC} = 4.5$ to $5.5V$	$0.8 * V_{CC}$	–	–	$0.8 * V_{CC}$	–	
V_{IL}	LOW level Input voltage RS input	$V_{CC} = 1.2V$	–	–	0.2	–	0.2	V
		$V_{CC} = 2.0V$	–	–	0.4	–	0.4	
		$V_{CC} = 2.7$ to $3.6V$	–	–	0.5	–	0.5	
		$V_{CC} = 4.5$ to 5.5	–	–	$0.2 * V_{CC}$	–	$0.2 * V_{CC}$	
V_{OH}	HIGH level output voltage; R_{TC} output	$V_{CC} = 1.2V$; RS = GND and MR = GND; $-I_O = 3.4mA$	–	–	–	–	–	V
		$V_{CC} = 2.0V$; RS = GND and MR = GND; $-I_O = 3.4mA$	–	–	–	–	–	
		$V_{CC} = 2.7V$; RS = GND and MR = GND; $-I_O = 3.4mA$	–	–	–	–	–	
		$V_{CC} = 3.0V$; RS = GND and MR = GND; $-I_O = 3.4mA$	2.40	2.82	–	2.20	–	
		$V_{CC} = 4.5V$; RS = GND and MR = GND; $-I_O = 3.4mA$	–	–	–	–	–	

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SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
V _{OH}	HIGH level output voltage; R _{TC} output	V _{CC} = 1.2V; RS = V _{CC} and MR = V _{CC} ; -I _O = 0.8mA	-	-	-	-	-	V
		V _{CC} = 2.0V; RS = V _{CC} and MR = V _{CC} ; -I _O = 0.8mA	-	-	-	-	-	
		V _{CC} = 2.7V; RS = V _{CC} and MR = V _{CC} ; -I _O = 0.8mA	-	-	-	-	-	
		V _{CC} = 3.0V; RS = V _{CC} and MR = V _{CC} ; -I _O = 0.8mA	2.40	2.82	-	2.20	-	
		V _{CC} = 4.5V; RS = V _{CC} and MR = V _{CC} ; -I _O = 0.8mA	-	-	-	-	-	
V _{OH}	HIGH level output voltage; R _{TC} output	V _{CC} = 1.2V; RS = GND and MR = GND; -I _O = 100μA	1.0	1.2	-	1.0	-	V
		V _{CC} = 2.0V; RS = GND and MR = GND; -I _O = 100μA	1.8	2.0	-	1.8	-	
		V _{CC} = 2.7V; RS = GND and MR = GND; -I _O = 100μA	-	-	-	-	-	
		V _{CC} = 3.0V; RS = GND and MR = GND; -I _O = 100μA	2.8	3.0	-	2.8	-	
		V _{CC} = 4.5V; RS = GND and MR = GND; -I _O = 100μA	-	-	-	-	-	
V _{OH}	HIGH level output voltage; R _{TC} output	V _{CC} = 1.2V; RS = V _{CC} and MR = V _{CC} ; -I _O = 100μA	1.0	1.2	-	1.0	-	V
		V _{CC} = 2.0V; RS = V _{CC} and MR = V _{CC} ; -I _O = 100μA	1.8	2.0	-	1.8	-	
		V _{CC} = 2.7V; RS = V _{CC} and MR = V _{CC} ; -I _O = 100μA	-	-	-	-	-	
		V _{CC} = 3.0V; RS = V _{CC} and MR = V _{CC} ; -I _O = 100μA	2.8	3.0	-	2.8	-	
		V _{CC} = 4.5V; RS = V _{CC} and MR = V _{CC} ; -I _O = 100μA	-	-	-	-	-	
V _{OH}	HIGH level output voltage; C _{TC} output	V _{CC} = 1.2V; RS = V _{IH} and MR = V _{IL} ; -I _O = 3.8mA	-	1.2	-	-	-	V
		V _{CC} = 2.0V; RS = V _{IH} and MR = V _{IL} ; -I _O = 3.8mA	-	-	-	-	-	
		V _{CC} = 2.7V; RS = V _{IH} and MR = V _{IL} ; -I _O = 3.8mA	-	-	-	-	-	
		V _{CC} = 3.0V; RS = V _{IH} and MR = V _{IL} ; -I _O = 3.8mA	2.40	2.82	-	2.20	-	
		V _{CC} = 4.5V; RS = V _{IH} and MR = V _{IL} ; -I _O = 3.8mA	-	-	-	-	-	
V _{OH}	HIGH level output voltage; except R _{TC} output	V _{CC} = 1.2V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 100μA	1.0	1.2	-	1.0	-	V
		V _{CC} = 2.0V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 100μA	1.8	2.0	-	1.8	-	
		V _{CC} = 2.7V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 100μA	-	-	-	-	-	
		V _{CC} = 3.0V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 100μA	2.8	3.0	-	2.8	-	
		V _{CC} = 4.5V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 100μA	-	-	-	-	-	

14-stage binary ripple counter with oscillator

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SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
V _{OH}	HIGH level output voltage; except R _{TC} and C _{TC} outputs	V _{CC} = 1.2V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 6mA	-	-	-	-	-	V
		V _{CC} = 2.0V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 6mA	-	-	-	-	-	
		V _{CC} = 2.7V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 6mA	-	-	-	-	-	
		V _{CC} = 3.0V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 6mA	2.40	2.82	-	2.20	-	
		V _{CC} = 4.5V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 6mA	-	-	-	-	-	
V _{OL}	LOW level output voltage; R _{TC} output	V _{CC} = 1.2V; RS = V _{CC} and MR = GND; -I _O = 3.4mA	-	-	-	-	-	V
		V _{CC} = 2.0V; RS = V _{CC} and MR = GND; -I _O = 3.4mA	-	-	-	-	-	
		V _{CC} = 2.7V; RS = V _{CC} and MR = GND; -I _O = 3.4mA	-	-	-	-	-	V
		V _{CC} = 3.0V; RS = V _{CC} and MR = GND; -I _O = 3.4mA	-	0.25	0.40	-	0.50	
		V _{CC} = 4.5V; RS = V _{CC} and MR = GND; -I _O = 3.4mA	-	-	-	-	-	
V _{OL}	LOW level output voltage; R _{TC} output	V _{CC} = 1.2V; RS = V _{CC} and MR = GND; -I _O = 100μA	-	0	0.2	-	0.2	V
		V _{CC} = 2.0V; RS = V _{CC} and MR = GND; -I _O = 100μA	-	0	0.2	-	0.2	
		V _{CC} = 2.7V; RS = V _{CC} and MR = GND; -I _O = 100μA	-	-	-	-	-	
		V _{CC} = 3.0V; RS = V _{CC} and MR = GND; -I _O = 100μA	-	0	0.2	-	0.2	
		V _{CC} = 4.5V; RS = V _{CC} and MR = GND; -I _O = 100μA	-	-	-	-	-	
V _{OL}	LOW level output voltage; C _{TC} output	V _{CC} = 1.2V; RS = V _{IH} and MR = V _{IL} ; -I _O = 3.8mA	-	-	-	-	-	V
		V _{CC} = 2.0V; RS = V _{IH} and MR = V _{IL} ; -I _O = 3.8mA	-	-	-	-	-	
		V _{CC} = 2.7V; RS = V _{IH} and MR = V _{IL} ; -I _O = 3.8mA	-	-	-	-	-	
		V _{CC} = 3.0V; RS = V _{IH} and MR = V _{IL} ; -I _O = 3.8mA	-	0.25	0.40	-	0.50	
		V _{CC} = 4.5V; RS = V _{IH} and MR = V _{IL} ; -I _O = 3.8mA	-	-	-	-	-	
V _{OL}	LOW level output voltage; except R _{TC} output	V _{CC} = 1.2V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 100μA	-	0	0.2	-	0.2	V
		V _{CC} = 2.0V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 100μA	-	0	0.2	-	0.2	
		V _{CC} = 2.7V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 100μA	-	-	-	-	-	
		V _{CC} = 3.0V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 100μA	-	0	0.2	-	0.2	
		V _{CC} = 4.5V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 100μA	-	-	-	-	-	

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SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
V _{OL}	HIGH level output voltage; except R _{TC} and C _{TC} outputs	V _{CC} = 1.2V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 6mA	-	-	-	-	-	V
		V _{CC} = 2.0V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 6mA	-	-	-	-	-	
		V _{CC} = 2.7V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 6mA	-	0.25	0.40	-	0.50	
		V _{CC} = 3.0V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 6mA	-	-	-	-	-	
		V _{CC} = 4.5V; V _I = V _{IH} and V _I = V _{IL} ; -I _O = 6mA	-	-	-	-	-	
I _I	Input leakage current	V _{CC} = 5.5V; V _I = V _{CC} or GND	-	-	1.0	-	1.0	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0	-	-	20	-	160	μA
	Quiescent supply current	V _{CC} = 5.5V; V _I = V _{CC} or GND; I _O = 0	-	-	-	-	80	
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0	-	-	500	-	850	μA

NOTE:1. All typical values are measured at T_{amb} = 25°C.**AC CHARACTERISTICS**GND = 0V; t_r = t_f = 2.5ns; C_L = 50pF; R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS -40 to +85 °C			LIMITS -40 to +125 °C		UNIT
				V _{CC} (V)	MIN	TYP ¹	MAX	MIN	
t _{PHL} /t _{PLH}	Propagation delay RS to Q ₃	Figures 6, 8	1.2	-	180	-	-	-	ns
			2.0	-	52	84	-	105	
			2.7	-	42	66	-	83	
			3.0 to 3.6	-	33 ²	53	-	66	
			4.5 to 5.5	-	24	39	-	49	
t _{PHL} /t _{PLH}	Propagation delay Q _n to Q _{n+1}	Figures 7, 8	1.2	-	40	-	-	-	ns
			2.0	-	14	23	-	29	
			2.7	-	10	16	-	20	
			3.0 to 3.6	-	8 ²	13	-	16	
			4.5 to 5.5	-	6	9	-	11	
t _{PHL}	Propagation delay MR to Q _n	Figures 7, 8	1.2	-	100	-	-	-	ns
			2.0	-	29	46	-	58	
			2.7	-	24	39	-	49	
			3.0 to 3.6	-	19 ²	31	-	39	
			4.5 to 5.5	-	14	23	-	29	
t _w	Clock pulse width RS; HIGH or LOW	Figure 6	2.0	34	9	-	38	-	ns
			2.7	25	6	-	30	-	
			3.0 to 3.6	20	5	-	24	-	
			4.5 to 5.5	16	4	-	20	-	
t _w	Master reset pulse width MR; HIGH	Figure 7	2.0	34	10	-	38	-	ns
			2.7	25	8	-	30	-	
			3.0 to 3.6	20	6	-	24	-	
			4.5 to 5.5	16	4	-	20	-	

14-stage binary ripple counter with oscillator

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SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS -40 to +85 °C			LIMITS -40 to +125 °C		UNIT
			V _{CC} (V)	MIN	TYP ¹	MAX	MIN	MAX	
t _{rem}	Removal time MR to RS	Figure 7	2.0	29	18	–	37	–	ns
			2.7	26	16	–	32	–	
			3.0 to 3.6	18	11	–	23	–	
			4.5 to 5.5	12	7	–	15	–	
f _{max}	Maximum clock pulse frequency	Figure 6	2.0	14	40	–	9	–	MHz
			2.7	19	70	–	12	–	
			3.0 to 3.6	24	90	–	15	–	
			4.5 to 5.5	30	100	–	19	–	

NOTE:

Unless otherwise stated, all typical values are at T_{amb} = 25°C.

1. Typical value measured at V_{CC} = 3.3V.
2. Typical value measured at V_{CC} = 5.0V.

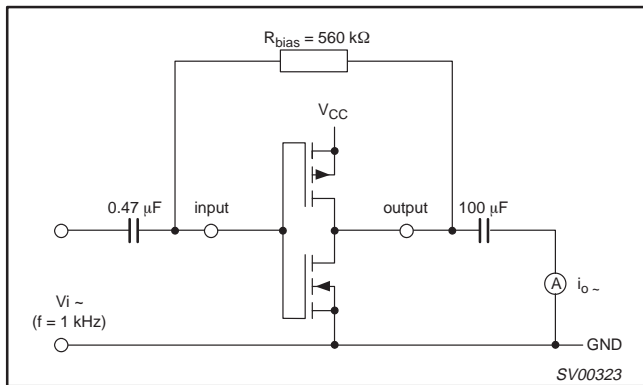


Figure 1.

Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Figure 2); MR = LOW.

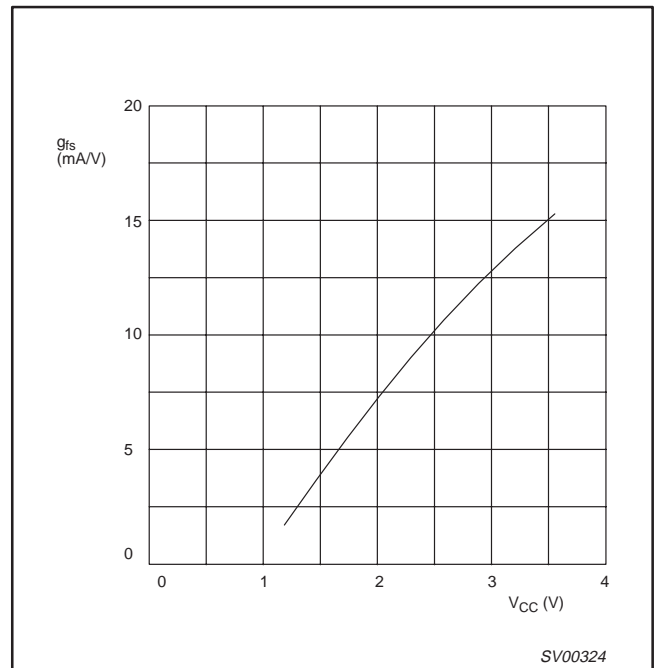


Figure 2.

Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25°C.

14-stage binary ripple counter with oscillator

74LV4060

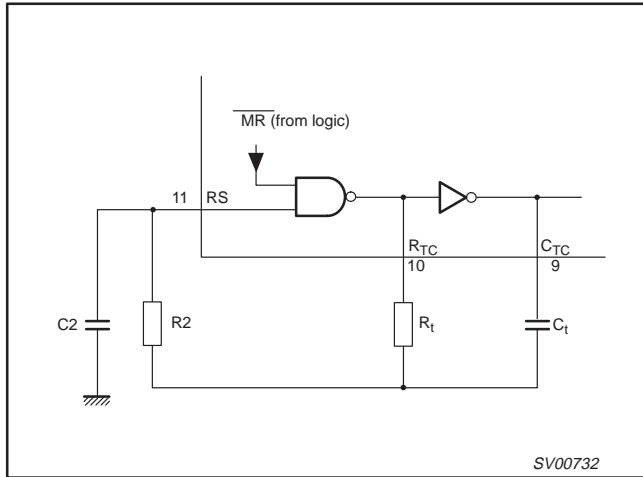


Figure 3.

Example of an RC oscillator. Typical formula for oscillator frequency:

$$f_{OSC} = \frac{1}{2.5 \times R_1 \times C_1}$$

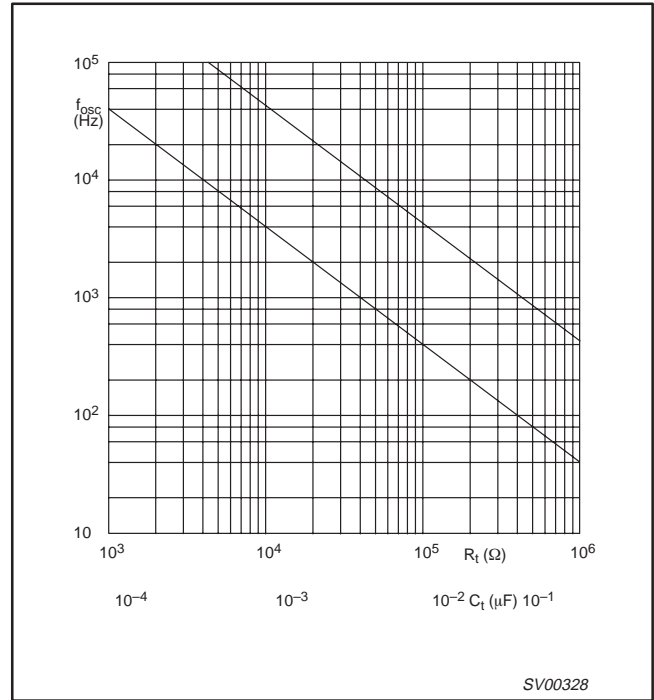


Figure 4.

RC oscillator frequency as a function of R_1 and C_1 at $V_{CC} = 1.2$ to 3.6 V; $T_{amb} = 25^\circ\text{C}$.
 C_1 curve at $R_1 = 100$ k Ω ; $R_2 = 200$ k Ω .
 R_1 curve at $C_1 = 1$ nF; $R_2 = 2 \times R_1$.

TIMING COMPONENTS LIMITATIONS

The oscillator frequency is mainly determined by $R_1 \cdot C_1$, provided $R_2 \approx 2R_1$ and $R_2 \cdot C_2 \ll R_1 \cdot C_1$. The function of R_2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_1 must be larger than the inherent stray capacitance. R_1 must be larger than the 'ON' resistance in series with it, which typically is 280 Ω at $V_{CC} = 1.2$ V, 130 Ω at $V_{CC} = 2.0$ V and 100 Ω at $V_{CC} = 3.0$ V. The recommended values for these components to maintain agreement with the typical oscillation formula are: $C_1 > 50$ pF, up to any practical value, 10 k $\Omega < R_1 < 1$ M Ω . In order to avoid start-up problems, $R_1 \geq 1$ k Ω .

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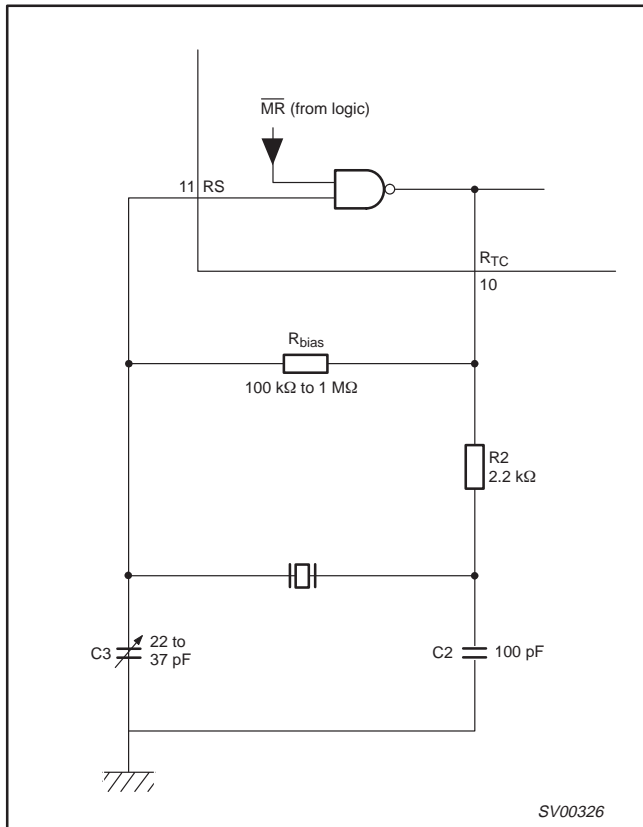


Figure 5. External components connection for a typical crystal oscillator

R2 is the power limiting resistor. For starting and maintaining oscillation, a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.

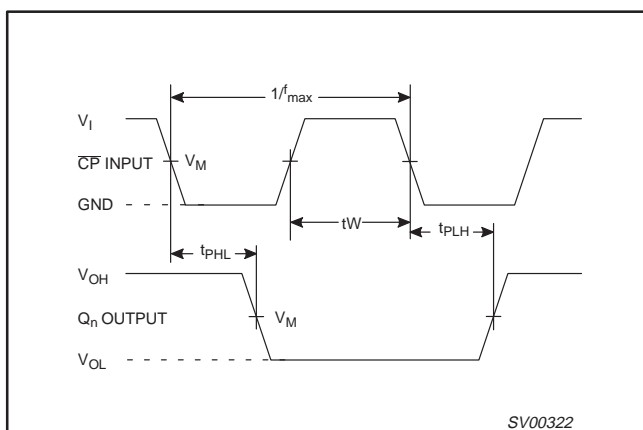


Figure 6.

Waveforms showing the clock (RS) to output (Q_3) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

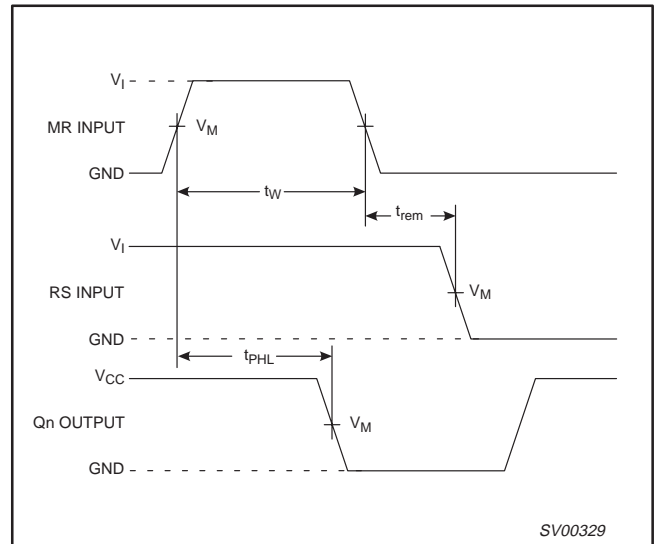


Figure 7.

Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (RS) removal time.

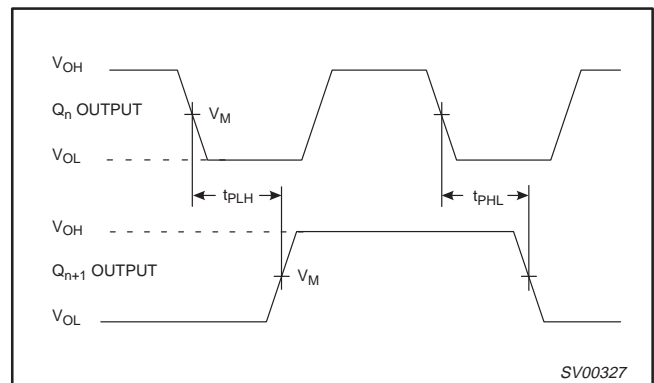


Figure 8.

Waveforms showing the output Q_n to output $n + 1$ propagation delays.

NOTES:

1. $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$ and $\leq 3.6 \text{ V}$
 $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7 \text{ V}$ and $\geq 4.5 \text{ V}$.
2. V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

14-stage binary ripple counter with oscillator

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TEST CIRCUIT

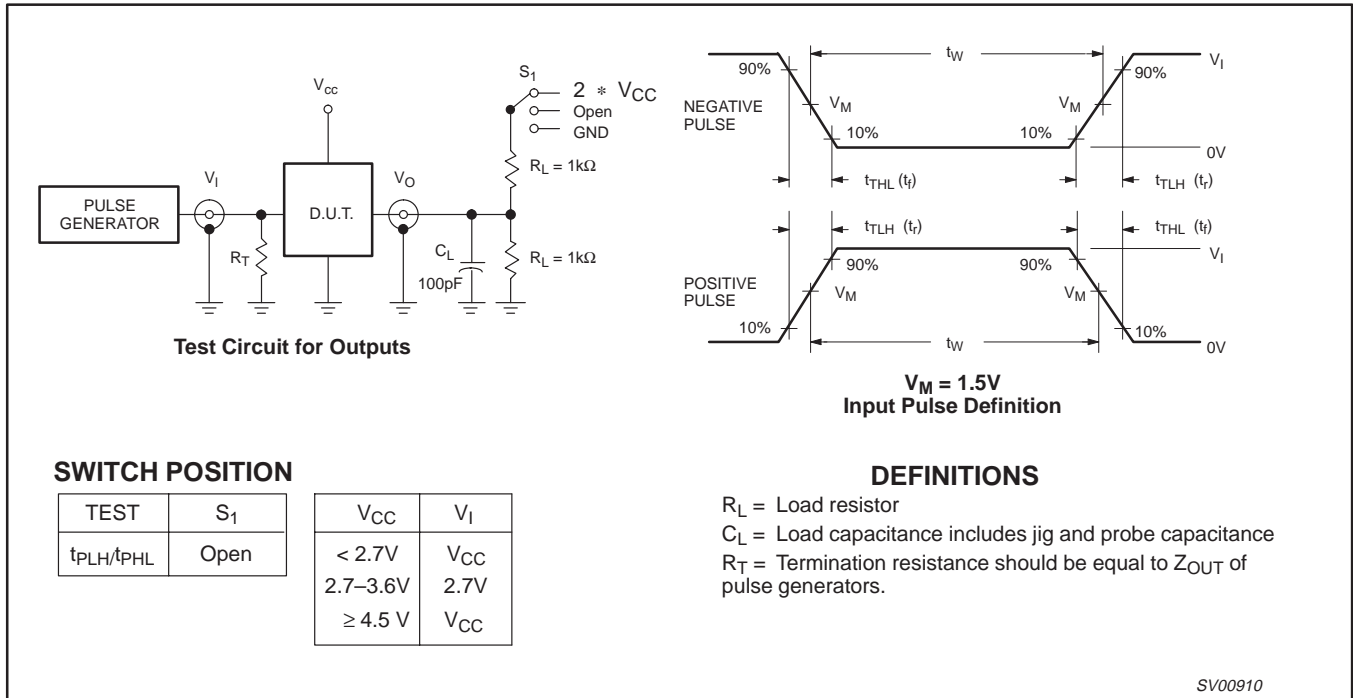


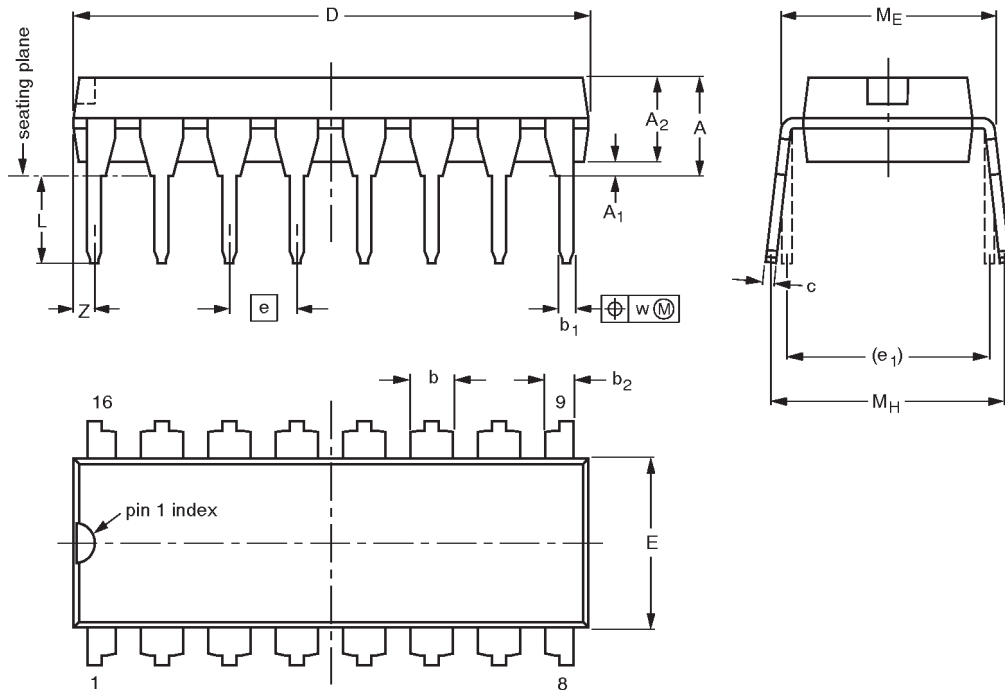
Figure 9. Load circuitry for switching times.

14-stage binary ripple counter with oscillator

74LV4060

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

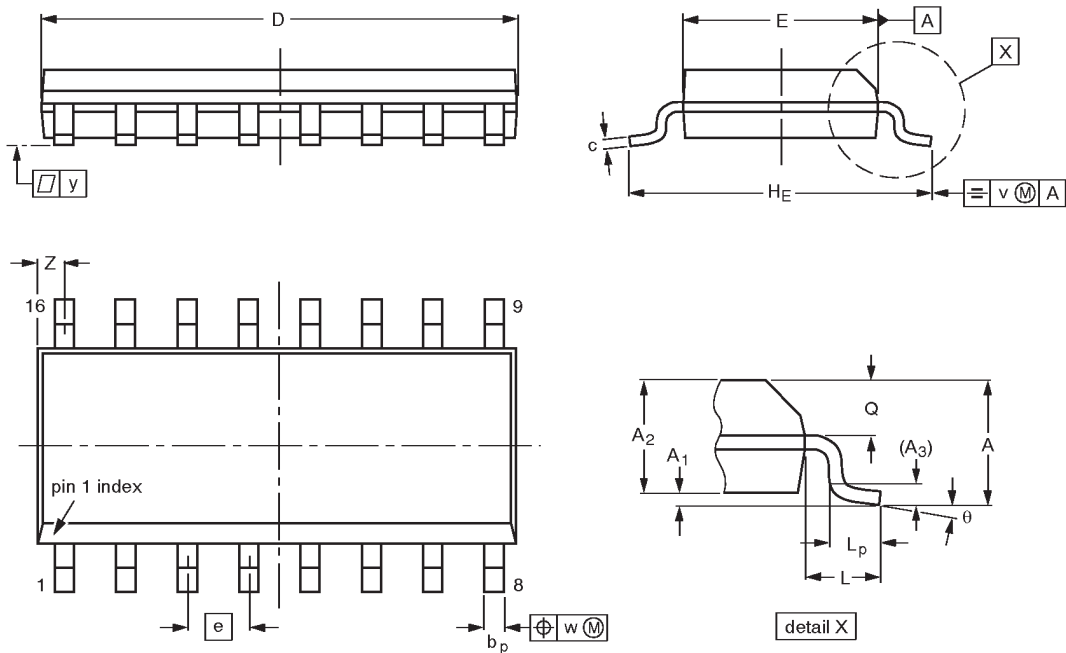
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

14-stage binary ripple counter with oscillator

74LV4060

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

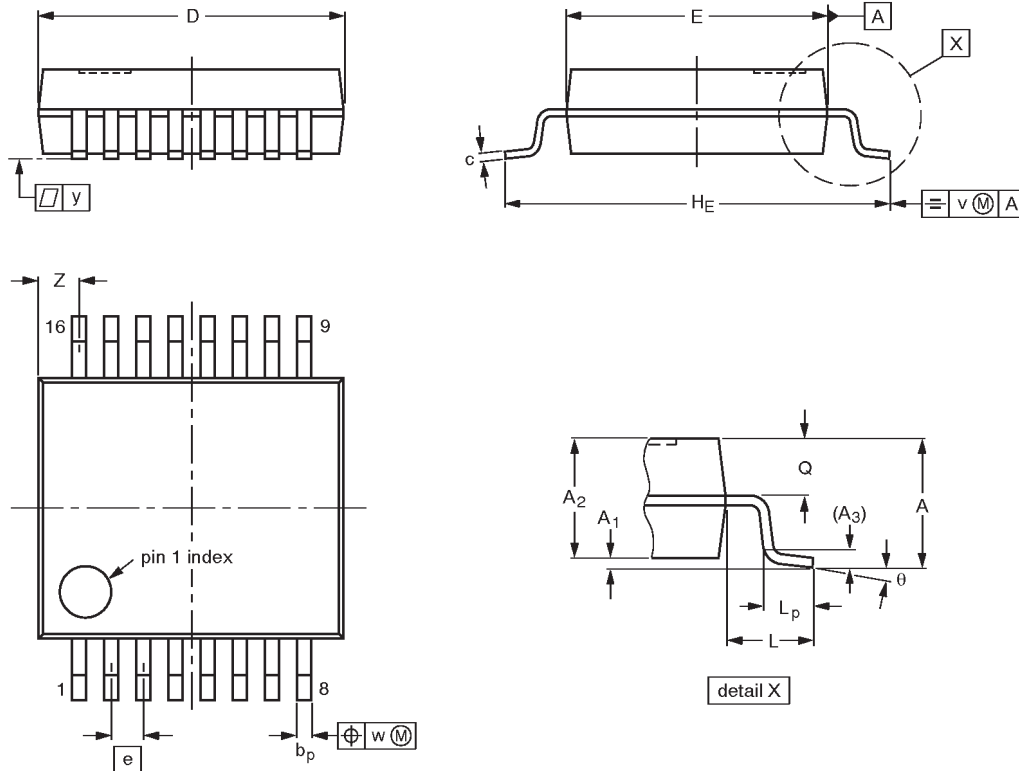
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				91-08-13 95-01-23

14-stage binary ripple counter with oscillator

74LV4060

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

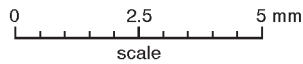
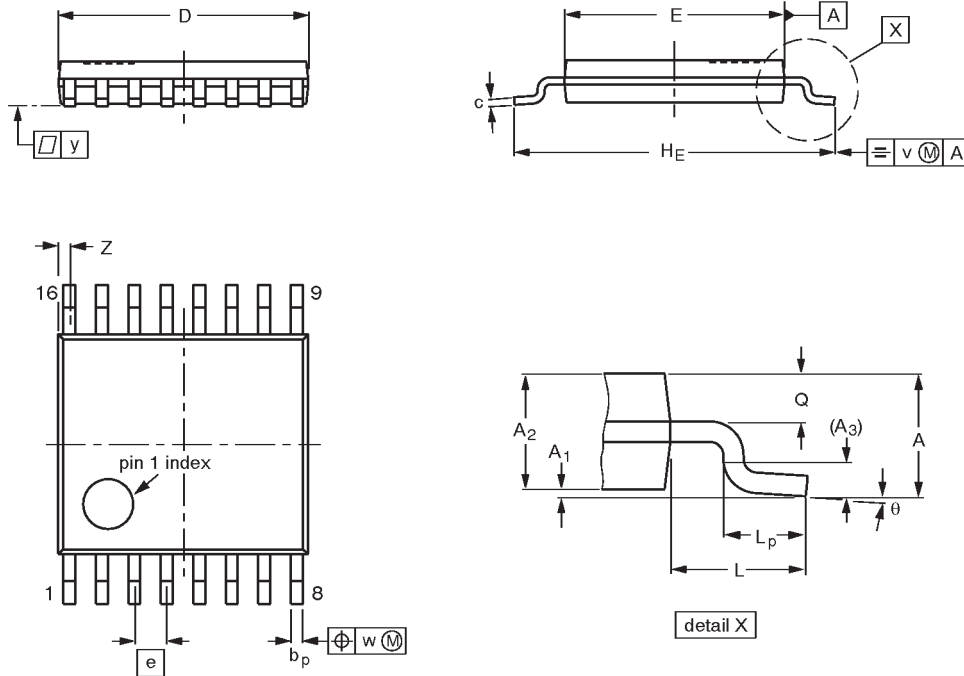
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14- 95-02-04

14-stage binary ripple counter with oscillator

74LV4060

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

14-stage bunary ripple counter with oscillator

74LV4060

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Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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